1. A magnitude content addressable memory (MCAM) comprising a plurality of MCAM cells, wherein a cell of the plurality of MCAM cells comprises:

a first memory cell for storing a data value; and

a magnitude comparator coupled to the first memory cell and operable to receive a comparison value and the data value as inputs to produce first and second magnitude signals as outputs;

wherein the first magnitude signal indicates if the comparison value is greater than the data value and the second magnitude signal indicates if the comparison value is less than the data value.

2. A content addressable memory in accordance with claim 1, wherein the magnitude comparator is further responsive to a previous first magnitude signal and a previous second magnitude signal output from a previous MCAM cell and wherein the previous first magnitude signal is output as the first magnitude signal and the previous second magnitude signal is output as the second magnitude signal when the data value and the comparison values are equal.

3. A content addressable memory in accordance with claim 2, wherein the MCAM cell further comprises a second memory cell for storing a mask bit and wherein the magnitude comparator is controlled by the mask value to pass the previous first

magnitude signal as the first magnitude signal and the previous second magnitude signal as the second magnitude signal when the mask bit has a predetermined value.

4. A content addressable memory in accordance with claim 2, wherein the magnitude comparator comprises:

a first logic circuit producing as output a match signal indicative of whether or not the data value and the comparison value match; and

a second logic circuit, responsive to the match signal, the previous first magnitude signal and the previous second magnitude signal and producing the first and second magnitude signals as output.

5. A content addressable memory in accordance with claim 4, wherein the first logic circuit comprises:

a first AND gate having the data value and the comparison values as inputs;

a second AND gate having the complement of the data value and the complement of the comparison values as inputs; and

a NOR gate having the output of the first and second AND gate as inputs and producing the match value as output.

6. A content addressable memory in accordance with claim 5, further comprising a second memory cell for storing a mask value, wherein the NOR gate is a controlled NOR gate controlled by mask value.

7. A content addressable memory in accordance with claim 4, wherein the second logic circuit comprises:

a first transmission gate controlled by the match signal and operable to pass the first previous magnitude signal as the first magnitude signal when the data value and comparison values match;

a second transmission gate controlled by the match signal and operable to pass the second previous magnitude signal as the second magnitude signal when the data value and comparison values match;

a third transmission gate controlled by the match signal and operable to pass the comparison value as the first magnitude signal when the data value and comparison values do not match; and

a fourth transmission gate controlled by the match signal and operable to pass the data value as the second magnitude signal when the data value and comparison values do not match.

8. A content addressable memory in accordance with claim 7, wherein at least one of the first, second, third and fourth transmission gates comprises a p-channel transistor and an n-channel resistor and is controlled by the match signal and it complement.

9. A content addressable memory in accordance with claim 1, wherein the plurality of MCAM cells are configured as at least one MCAM cell group having a series arrangement, and wherein the comparator of an MCAM cell in the at least one group is responsive to the first and second magnitude signals of a preceding MCAM cell in the series arrangement.

10. A content addressable memory in accordance with claim 9, wherein the first MCAM cell of an MCAM group is operable to store the least significant bit of a data word and last MCAM cell of the MCAM group is operable to store the most significant word of the data word.

11. A content addressable memory in accordance with claim 9, wherein the plurality of MCAM cells are configured as an arrangement of at least two MCAM cell groups and further comprising:

a second stage comparator responsive to the first and second magnitude signal of the last cell in a first MCAM cell group and responsive to the first and second magnitude signal of the last cell in a second MCAM cell group and

operable to produce first and second magnitude signals.

12. A content addressable memory in accordance with claim 11, wherein the plurality of MCAM cells are configured as an array of at least two MCAM cell groups, each row of the array being a series arrangement of MCAM groups connected by second stage comparators and the rows being connected in parallel by second stage comparators.

13. A content addressable memory in accordance with claim 11, wherein the second stage comparator comprises:

a first NOR gate responsive to the first magnitude signal of the first MCAM cell group and the first magnitude signal of the second MCAM cell group to produce a first comparison signal;

a second NOR gate responsive to the second magnitude signal of the first MCAM cell group and the second magnitude signal of the second MCAM cell group to produce a second comparison signal;

a third NOR gate responsive to the second magnitude signal of the first MCAM cell group and the first comparison signal to produce a first output magnitude signal; and

a fourth NOR gate responsive to the first magnitude signal of the first MCAM cell group and the second comparison signal to produce a second output magnitude signal.

14. A content addressable memory in accordance with claim 1, wherein the first memory is an SRAM.

15. A content addressable memory in accordance with claim 14, further comprising:

a write line coupled to the SRAM;

a first bit line coupled to the SRAM for carrying a true data signal to be stored in the SRAM; and

a second bit line coupled to the SRAM for carrying a complementary data signal to be stored in the SRAM.

16. A content addressable memory in accordance with claim 9, further comprising a signal booster, operable to boost the level at a first or second magnitude signal and thereby avoid signal degradation.

17. A content addressable memory comprising:

at least one group of MCAM cells, each MCAM cell comprising a data memory for storing a bit of a data word and a magnitude comparator for comparing the bit of the data word to a corresponding bit of a comparison word;

a word line for the group of MCAM cells;

a plurality of data bit lines, one for each MCAM cell in the group of MCAM cells, for supplying bits of the data word to the MCAM cells;

a plurality of comparison bit lines, one for each MCAM cell in the group of MCAM cells, for supplying bits of the comparison word to the MCAM cells,

wherein the magnitude comparators of the MCAM cells are connected in a series arrangement and are operable to produce a first magnitude signal indicating whether the comparison word is greater than the data word and a second magnitude signal indicating whether the comparison word is less than the data word.

18. A content addressable memory in accordance with claim 17, wherein each MCAM cell further comprises mask memory for storing a mask value and wherein the magnitude comparator is a controlled magnitude comparator controlled by the

mask value.

19. A content addressable memory in accordance with claim 17, wherein the at least one group of MCAM cells include a first MCAM cell group for storing a first sub-word of the data word and a second MCAM cell group for storing a second sub-word of the data word and further comprising a second stage comparator, responsive to the first and second magnitude signals and the first MCAM cell group and the first and second magnitude signals and the second MCAM cell group.

20. A content addressable memory in accordance with claim 19, wherein the second stage comparator comprises:

a first NOR gate responsive to the first magnitude signal of the first MCAM cell group and the first magnitude signal of the second MCAM cell group to produce a first comparison signal;

a second NOR gate responsive to the second magnitude signal of the first MCAM cell group and the second magnitude signal of the second MCAM cell group to produce a second comparison signal;

a third NOR gate responsive to the second magnitude signal of the first MCAM cell group and the first comparison signal to produce a first output magnitude signal; and

a fourth NOR gate responsive to the first magnitude signal of the first MCAM cell group and the second comparison signal to produce a second output magnitude signal.

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21. A method of comparing a plurality of bits of a comparison word and a data word in a magnitude content addressable memory comprising a sequence of MCAM cells, the method comprising:

storing each bit of the data word in a data memory of an MCAM cell of the sequence of MCAM cells, the least significant bit of the data word being stored in a first MCAM cell of the sequence of MCAM cells;

supplying signals representing the least significant bit of the data word and a corresponding least significant bit of the comparison word to a comparator of the first MCAM cell to determine if the least significant bit of the comparison word is greater than or less than the least significant bit of the data word;

outputting from the first MCAM cell a first magnitude signal indicating whether the least significant bit of the comparison word is greater than the least significant bit of the data word;

outputting from the first MCAM cell a second magnitude signal indicating whether the least significant bit of the comparison word is less than the least significant bit of the data word; and

for each subsequent bit of the plurality of bits, the subsequent bit of the data word being stored in a data memory of a current MCAM cell:

supplying signals representing the bit of the data word and the corresponding bit of the comparison word to a logic circuit of the current MCAM cell to determine if the bit of the comparison word matches of the bit of the data word;

if the bit of the comparison word matches the bit of the data word:

outputting the first magnitude signal of the preceding MCAM cell as the first magnitude signal of the current MCAM cell;

outputting the second magnitude signal of the preceding MCAM cell as the second magnitude signal of the current MCAM cell;

otherwise:

outputting the signal representing the comparison bit as the first magnitude signal of the current MCAM cell; and

outputting the signal representing the data bit as the second magnitude signal of the current MCAM cell.

22. A method in accordance with claim 21, further comprising:

storing a mask value in a mask memory of an MCAM cell; and

if the mask value indicates that the associated data bit in the MCAM cell is to be masked:

outputting the first magnitude signal of the preceding MCAM cell as the first magnitude signal of the current MCAM cell;

outputting the second magnitude signal of the preceding MCAM cell as the second magnitude signal of the current MCAM cell.

23. A method in accordance with claim 21, wherein outputting the first magnitude signal of the preceding MCAM cell as the first magnitude signal of the current MCAM cell comprises:

supplying the first magnitude signal of the preceding MCAM cell to the input of a transmission gate;

supplying a match signal, indicative of whether the comparison word matches the bit of the data word to a first transistor of the transmission gate;

supplying a complement of the match signal to a second transistor of the transmission gate; and

outputting the output from the transmission gate.

24. A method in accordance with claim 21, wherein outputting the signal representing the comparison bit as the first magnitude signal of the current MCAM cell comprises:

supplying the signal representing the comparison bit to the input of a transmission gate;

supplying a match signal, indicative of whether the comparison word matches the bit of the data word to a first transistor of the transmission gate;

supplying a complement of the match signal to a second transistor of the transmission gate; and

outputting the output from the transmission gate.

25. A method in accordance with claim 21, wherein outputting the second magnitude signal of the preceding MCAM cell as the second magnitude signal of the current MCAM cell comprises:

supplying the second magnitude signal of the preceding MCAM cell to the input of a transmission gate;

supplying a match signal, indicative of whether the comparison word matches the bit of the data word to a first transistor of the transmission gate;

supplying a complement of the match signal to a second transistor of the transmission gate; and

outputting the output from the transmission gate.

26. A method in accordance with claim 21, wherein outputting the signal representing the data bit as the second magnitude signal of the current MCAM cell comprises:

supplying the signal representing the data bit to the input of a transmission gate;

supplying a match signal, indicative of whether the comparison word matches the bit of the data word to a first transistor of the transmission gate;

supplying a complement of the match signal to a second transistor of the transmission gate; and

outputting the output from the transmission gate.

27. A method in accordance with claim 21, wherein the first magnitude signal CRYG is computed in accordance the truth table:

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| DATAT | COMPT | CRYGP | CRYG |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

and wherein the second magnitude signal CRYL is computed in accordance the truth table:

| INPUTS | | | OUTPUTS |
|---|---|---|---|
| DATAT | COMPT | CRYLP | CRYL |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

where DATAT is the data value, COMPT is the comparison value, CRYGP is the previous first magnitude signal and CRYLP is the previous second magnitude signal.

28. A method in accordance with claim 21, wherein the sequence of MCAM cells comprises a first group of MCAM cells and a second group of MCAM cells, the method further comprising:

supplying the first and second magnitude signals of the last MCAM cell of the first group of MCAM cells to a second stage comparator;

supplying the first and second magnitude signals of the last MCAM cell of the second group of MCAM cells to a second stage comparator;

outputting a first magnitude signal from the second stage comparator, indicative of whether a data word stored in the first and second groups of MCAM cells is greater than the comparison word; and

outputting a second magnitude signal from the second stage comparator, indicative of whether the data word stored in the first and second groups of MCAM cells is less than the comparison word.

29. A method in accordance with claim 21, wherein the first magnitude signal CRYGN output from the second stage is computed in accordance the truth table:

| INPUTS | | | OUTPUT |
|---|---|---|---|
| CRYG | CRYGP | CRYL | CRYGN |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

and where the second magnitude signal CRYLN output from the second stage is

computed in accordance the truth table:

| INPUTS | | | OUTPUT |
|---|---|---|---|
| CRYL | CRYLP | CRYG | CRYLN |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

where CRYGP is the first magnitude signal output from the first group of MCAM cells, CRYLP is the previous second magnitude signal output from the first group of MCAM cells, CRYG is the first magnitude signal output from the second group of MCAM cells and CRYL is the previous second magnitude signal output from the second group of MCAM cells.

30. A method in accordance with claim 21, further comprising boosting the first and second magnitude signals between adjacent groups of MCAM cells.

31. A magnitude content addressable memory (MCAM) comprising a plurality of MCAM cells, wherein a cell of the plurality of MCAM cells comprises:

a first memory cell for storing a data value; and

comparison means, coupled to the first memory cell and operable to receive a comparison value and the data value as inputs, for generating first and second magnitude signals as outputs;

wherein the first magnitude signal indicates if the comparison value is greater than the data value and the second magnitude signal indicates if the comparison value is less than the data value.

32. A content addressable memory in accordance with claim 31, wherein the comparison means is further responsive to a previous first magnitude signal and a previous second magnitude signal output from a previous MCAM cell and wherein the previous first magnitude signal is output as the first magnitude signal and the previous second magnitude signal is output as the second magnitude signal when the data value and the comparison values are equal.

33. A content addressable memory in accordance with claim 32, wherein the MCAM cell further comprises a second memory cell for storing a mask bit and wherein the comparison means is controlled by the mask value to pass the previous first

magnitude signal as the first magnitude signal and the previous second magnitude signal as the second magnitude signal when the mask bit has a predetermined value.

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